REMARKS/ARGUMENTS

This amendment responds to the Office Action dated August 20, 2008, in which the Examiner rejected claims 1-28 under 35 U.S.C. § 103.

Applicants would like to thank the Examiner for the telephone interview on November 3, 2008, in which the Examiner agreed that the amended claims were distinguished over the cited prior art.

Attached to this Amendment is a Replacement sheet for Figure 9B to correct typographical errors. Support for the Amendment can be found in paragraph 0095 of the published application. Applicants respectfully request the Examiner approves the corrections.

As indicated above, claims 1, 6, 11, 18 and 25-28 have been amended in order to make explicit what is implicit in the claims. The amendment is unrelated to a statutory requirement for patentability.

Claim 1 claims a compression encoder, claim 6 claims a compression-encoding method, claim 11 claims a recorder and claim 18 claims a recording method. The compression encoder, compression method, recorder and recording method comprise dividing input first and second digital input signals, having frame rates different from each other into plural macro blocks for each frame. The macro blocks are then rearranged in each frame into groups based on the frame rate and macro block units are created for every group by a shuffling section. The digital image signals for every macro block unit are then compression encoded. The macro blocks of the first digital image signal are rearranged such that an output order of the macro block units of the first digital image signals after compression-encoding is equivalent to the output order of the macro blocks units of the second digital image signal.

By having a shuffling section which rearranges the macro blocks in each frame into groups based on the frame rate and creates macro block units for every group such that the macro blocks of the first digital image signals are rearranged such that an output order of the macro block units of the first digital image signals after compression-encoding is equivalent to the output order of the macro blocks of the second digital image signals as claimed in claims 1, 6, 11 and 18, the claimed invention provides a compression encoder, compression encoder method, recorder and recording method in which the number of decoders necessary for half-speed reproduction of the first image signal can be reduced so that deterioration of resolution can be restricted without needing an interpolation processing. The prior art does not show, teach or suggest the invention as claimed in claims 1, 6, 11 and 18.

Claim 25 claims a compression encoder, claim 26 claims a compression-encoding method, claim 27 claims a recorder and claim 28 claims a recording method. The compression encoder, compression-encoding method, recorder and recording method include dividing first and second digital image signals into plural macro blocks for each frame. The plural macro blocks in each frame of the second digital image signal are rearranged into groups based on frame rate and macro block units are created for every group. The second digital image signals are rearranged into a layout of macro block units after compression-encoding which is equivalent to that of the first digital image signal. The rearranged plural macro blocks are then compression-encoded.

By rearranging the plural macro blocks into groups based on frame rate and creating macro block units for every group such that a layout of macro block units after compression-encoding is equivalent for the first and second image signals as claimed in claims 25-28, the

claimed invention provides a compression-encoder, compression-encoding method, recorder and recording method which requires no interpolation process when performing a half-speed reproduction so that resolution can be prevented from deteriorating. Furthermore, only one decoder is necessary during reproduction. The prior art does not show, teach or suggest the invention as claimed in claims 25-28.

Claims 1-2, 4, 6-7, 9, 11-14, 16, 18-21, 23 and 25-28 were rejected under 35 U.S.C. § 103 as being unpatentable over *Miller, et al.* (U.S. Patent No. 5,146,324), in view of *Katata, et al.* (U.S. Patent No. 6,714,591).

Miller, et al. appears to disclose a block shuffler 10 which accepts luminance data and chrominance data, partitions it into predetermined blocks of data and rearranges the data blocks within each field of video (Col. 5, lines 11-14). The block shuffler 10 rearranges the data into a time order corresponding to the physical blocks in the image and further scrambles the data by selecting blocks in an order other than the original sequence of the blocks in the image (Col. 6, line 68 – Col. 7, lines 1-4).

Thus, *Miller, et al.* merely discloses arranging data into a time order and scrambling the data. Nothing in *Miller, et al.* shows, teaches or suggests rearranging plural macro blocks in each frame into groups based upon frame rate as claimed in claims 1, 6, 11, 18 and 25-28. Rather, *Miller, et al.* only discloses arranging data into a time order since the data does not have different frame rates.

Additionally, since *Miller, et al.* merely discloses arranging data into a time order corresponding to the physical blocks in the image, nothing in *Miller, et al.* shows, teaches or suggests that an output order of the macro block units after compression-encoding is equivalent

to the output order of another digital image signal as claimed in claims 1, 6, 11, 18 and 25-28. Rather, *Miller, et al.* merely discloses rearranging data into a time order.

Katata, et al. appears to disclose coding a partial region (partial image) of an entire image in a first coding mode with coding the shaped data in the region so that it is possible to encode a partial region of a part image at a different frame rate than the other area (Col. 11, lines 7 – 10).

Thus, *Katata, et al.* merely discloses encoding different parts of an image at different frame rates. Nothing in *Katata, et al.* shows, teaches or suggests (a) rearranging plural macro blocks in each frame into groups based upon frame rate and (b) rearranging the macro blocks such that an output order of the macro block units after compression-encoding is equivalent to the output order of the macro block units of another digital image signal having a different frame rate as claimed in claims 1, 6, 11-18 and 25-28. Rather, *Katata, et al.* only discloses encoding a partial area of an image at a different frame rate than the other area.

A combination of *Miller, et al.* and *Katata, et al.* would merely suggest to arrange the data into a time order as taught by *Miller, et al.* and to encode different parts of the image at different frame rates as taught by *Katata, et al.* Thus, nothing in the combination of the references shows, teaches or suggests (a) rearranging plural macro blocks in each frame into groups based upon frame rate and (b) rearranging the macro blocks of a digital image signal such that an output order of the macro block units after compression-encoding is equivalent to the output order of the macro block units of another digital image signal as claimed in claims 1, 6, 11, 18 and 25-28. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claims 1, 6, 11, 18 and 25-28 under 35 U.S.C. § 103.

Claims 2, 4, 7, 9, 12-14, 16, 19-21 and 23 depend from claims 1, 6, 11 and 18 and recite additional features. Applicants respectfully submit that claims 2, 4, 7, 9, 12-14, 16, 19-21 and 23 would not have been obvious within the meaning of 35 U.S.C. § 103 over *Miller, et al.* and *Katata, et al.* at least for the reasons as set forth above. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claims 2, 4, 7, 9, 12-14 16, 19-21 and 23 under 35 U.S.C. § 103.

Claims 3, 8, 15 and 22 were rejected under 35 U.S.C. § 103 as being unpatentable over *Miller, et al.*, *Katata, et al.* in view of *Chen, et al.* (U.S. Publication No. 2003/0138051). Claims 5, 10, 17 and 24 were rejected under 35 U.S.C. § 103 as being unpatentable over *Miller, et al.*, *Katata, et al.* in view of *Porter, et al.* (U.S. Patent No. 7,227,900).

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. § 103. The claims have been reviewed in light of the Office Action and for reasons which will be set forth below, Applicants respectfully request the Examiner withdraws the rejection to the claims and allows the claims to issue.

As discussed above, since nothing in *Miller, et al.* and *Katata, et al.* show, teach or suggest the primary features as claimed in claims 1, 6, 11 and 18, Applicants respectfully submit that the combination of the primary references with the secondary reference to *Chen, et al.* or *Porter, et al.* will not overcome the deficiencies of the primary references. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claims 3, 5, 8, 10, 15, 17, 22 and 24 under 35 U.S.C. § 103.

The prior art of record, which is not relied upon, is acknowledged. The references taken singularly or in combination do not anticipate or make obvious the claimed invention.

Thus, it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

CONCLUSION

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is requested to contact, by telephone, the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to Deposit Account No. 50-0320.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 50-0320.

Respectfully submitted,

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